GALS Design for Nanoscale Digital Systems

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Outline

- Motivation
- Concept of the GALS/Synchronous Chip in 40 nm CMOS
- Chip Implementation
- Conclusions/Future Tasks
Motivation

- Recent advances in the area of the wireless communications pushed many new applications.

- There are several standards that are on the way (like IEEE 802.15.3) and requesting much higher datarates of 1 - 2 Gbps. For such high datarates it is foreseen to use the frequency bands in 60 GHz range.

- We have already developed BiCMOS RF transceiver compliant to 60 GHz band

- Currently this baseband supports datarates up to 1 Gbps but it is planned that the same architecture is the basis for higher datarates.

- GALS (Globally Asynchronous Locally Synchronous) methodology has been proposed as a solution for the system integration

  GALS methodology can affect also EMI properties of the digital systems
Possibilities and Competitors

- We have proposed the implementation of the hardware accelerator for 60 GHz communications, in order to evaluate the GALS technology on the complex demonstrator.

- GALS system can be implemented also using point-to-point GALS

- There were several point-to-point GALS chips implemented (99-05)

- There are also at least three GALS NoC implementation: NEXUS chip, and three LETI implementation, FAUST chip [2006], ALPIN chip [2008], MAGALI chip [2010].
Point-to-point vs. NoC GALS Approach in GALAXY Project

- Point-to-point GALS implementation in GALAXY project is challenging
  It will have significant impact, due to the real application field, applied technology, improved interfaces, low-EMI features

- In the last few years the community also working on GALS NoC system architectures and implementations
  Main "competitor", LETI, is focused on GALS NoC chip for wireless communications

- The real crossbenchmarking between the GALS NoC and sync NoC solution has never been made
Applicability of NoC to OFDM BB Processor

- OFDM baseband processor is optimized datapath structure with point-to-point structures inside and without the single bus. **Point-to-point processor architecture is optimal, and NoC brings no benefit.**

- Therefore, the implementation of NoC technology to the target baseband processor makes no sense!

- Modification of original synchronous target was considered to fit NoC needs is beyond the targets/ressources of the project and brings not acceptable additional risk.

- Therefore, we have concentrated on point-to-point GALS architecture. **GALS NoC test structures are also implemented to make sync-GALS NoC crossbenchmarking**
• We have planned to implement OFDM baseband transmitter in 60 GHz band

• Currently this processor is implemented in FPGA, achieving 1 Gbps throughput

• The goal is to increase the throughput with ASIC solution, reduce the power, and area

• It is very challenging to apply the GALS technology on the ‘state-of-the-art complex platform

  Most of the other GALS demonstrators were built using artificial systems without the real application
60 GHz OFDM PHY Parameters

- Main application scenario: HDTV video streaming
- Narrowband (FFT-BW: 400 MHz) and wideband (FFT-BW: 800 MHz) PHY mode defined
- Standard convolutional (171,133) codes used
- Application of parallel coding streams allows implementation with low digital clock frequency
- Modulation ranges from BPSK-1/2 to 64-QAM-3/4
To limit the required throughput rate of the decoder, the original data stream is splitted into several streams, which are encoded and interleaved separately.

- The streams are transmitted interleaved one after each other.

- A time division scheme is used where each OFDM data symbol is assigned to only one stream.
Hardware Structure of the Baseband Transmitter

Input control block → Scrambler → Symbol mapping

- encoder 1
- encoder 2
- encoder 12

Interface N_streams → 6

- interleaver 1
- interleaver 2
- interleaver 6

Subcarrier mapping and pilot insertion → Mapper → FFT 256 → Preamble insertion
Main Components - FFT

- Our OFDM scheme proposes application of 256-FFT. It is required to run FFT with clock frequency > 400 MHz.

- FFT is implemented with 4 X 64-FFT and 4-FFT. We process 4 samples in on clock cycle with 4 different FFT-64.

- Output 4 FFT streams are processed in a final 4-FFT stage.

- Such we can process samples arriving with 400 MSPS with a 100 MHz FFT. The price is paid with approximately 4-times increase in area.
Hardware Complexity in FPGA

<table>
<thead>
<tr>
<th>block</th>
<th>gates (Mil.)</th>
<th>slices</th>
<th>flip-flops</th>
<th>4-input LUT</th>
<th>BRAM</th>
<th>MULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx</td>
<td>7.8</td>
<td>12430</td>
<td>18069</td>
<td>16375</td>
<td>111</td>
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</tbody>
</table>

* Extracted from synthesis on Xilinx Virtex2P100
60 GHz Transceiver System

0.25 um SiGe BiCMOS Technology; Max data rate: 3.6 Gbit/s demonstrated
Main Goals to Achieve

• Crossbenchmarking sync-async GALS
  Compare design process
  Evaluate system integration with GALS approach
  Evaluate the design parameters (power, performance, etc.)

• High-performance GALS in a real application

• Low-EMI -> we have implemented low-EMI GALS circuits.

• GALS NoC evaluation -> covered by test structure
Moonrake Chip

- Moonrake chip is the first GALS chip produced using 40 nm CMOS process
- It consists of two different OFDM transmitter implementations
- Additionally it contains several NoC test structures
Implementation Details – Moonrake Chip

• The goal is to have parallel implementation
  1) Implementing synchronous baseband transmitter
  2) GALS version of baseband transmitter – pausable clocking, low-EMI

• We have planned for 136 signal pads + ~50-70 power/gnd pads
  That corresponds to 9mm² chip area

• It is challenging to design the complete baseband transmitter
  We have around 200 small/medium size RAM/ROM instances
  Complex DSP architectures are parallelized

• Target frequency is 160 MHz
  Dominated by pad frequency
Architecture of Moonrake Chip

Input FIFO

Data from MAC

GALS Tx

LC1  LC2  LC3  LC4  LC5  LC6

Synchronous Tx

BIST  PLL  JTAG  Clock control

Output Stage

Data to DAC
**GALSTOP** (GALS Transmitter)  
(GALS Tx has interfaces driven by synchronous GALS clk, however internally there are several GALS blocks that are triggered with pausable clocks generated from ring oscillators)

**clockcontrol**

- **PLL** (programmable over JTAG)
- **DIV/2**
- **clk26** (input ref 25 MHz)
- **clkp** (200 MHz)
- **MUX**
- **select PLL clock, PLL clock/2, or ref clock (DFT mode)**
- **local clocks generated in GALS blocks**
- **clk_outreg**
- **DIV/2**
- **div_clk**

**GALS Transmitter**

- **pausable clock 0**
- **pausable clock 1**
- **...**
- **pausable clock 5**

**Tx_top_final_new** (Synchronous Transmitter)

- **clock gating**
- **clock sync**
- **clk_sync**
- **WRCLK**

**INPUT_STAGE**

- **TOP_FIFO_2048X32**

**BIST_MODULEGALS**

**OUTPUT_STAGE**

**JTAG_TX**

**INPUT_STAGE TOP_FIFO_2048X32**

**BIST_MODULEGALS**

**OUTPUT_STAGE**

**JTAG_TX**
GALS Partitioning in Moonrake Chip

GALS BLOCK 1
- Pausible clock generator 1
- Input data FIFO
- Symbol mapping
- Universal scrambler
- GALS BLOCK 2
  - Interleaver [2:1]
  - Pausible clock generator 2
- GALS BLOCK 3
  - Interleaver [4:3]
  - Pausible clock generator 3
- GALS BLOCK 4
  - Interleaver [6:5]
  - Pausible clock generator 4
- GALS BLOCK 5
  - Pausible clock generator 5
- GALS BLOCK 6
  - Pausible clock generator 6
- Universal FEC encoder [12:1]
Port controllers
Design Structure of Moonrake Implementation

Area dominated by RAM structures (60-70%)

Equivalent gate count around 16 Mil. gates
Basic Info – Moonrake (IHP TX Chip, UNIBO Test Chip)

- **Moonrake Chip (IHP/UNIBO)**
  - Bondlib 55u pitch
  - Area $4000u\times 2250u = 9mm^2$
  - ~ 136 signal pins (IHP)
  - ~ 29 signal pins (UNIBO)
  - ~ 70 power pins (35 VDD/VSS pairs for core and ring supply)

This will be one of the most complex GALS chip implemented ever!
(comparison - ALPIN chip LETI, 65 nm, 11.5 mm$^2$ with pads,
MAGALI chip LETI, 65 nm, 32mm$^2$ with pads)
Moonrake Chip Floorplan

Final floorplan

NOC&PLL

GALS

Tx
Current Status & Next Steps

• Synthesis/Back-end of Moonrake is done

• We have implemented low-EMI GALS features in Moonrake chip

• GALS NoC evaluator is implemented also as a separate test structure.

• Taped-out 04/10

• Results will be available as planned 09/10

• Test specifications and test boards are under preparations.
**Main Final Demonstrator**

- System has to be finally applied in our 60 GHz demonstrator
Acknowledgement

- This work is funded by EC as part of our research in GALAXY project (GALS InterfAce for CompleX Digital SYstem Integration)
  www.galaxy-project.org