Design and Applications of Delay Locked Loop

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Delay elements and delay lines

Architecture and properties of DLL circuits, comparison with PLL

Linearization of analog delay element, three solutions

Application with delay elements and DLL circuits
Delay elements generate small delay time. Several delay elements connected in chain is **delay line** (used for larger delay time).
Digital delay lines are realized as a chain of elements with fixed delay value. The number of elements in a chain determines the amount of the delay.
Digital delay lines are controlled with:

- multiplexer,
- shift register and
- CMOS switch
Simple circuits with structure of inverter or buffer.

Control voltage change:

- DC operate point,
- impedance value in critical circuit’s node
It consists of:

- two inverters stage
- bias circuit

Transistors $M_3$ & $M_4$ limited charging/ discharging current of parasite output capacitance.

\[ t_d = \frac{C_L \cdot V_{dd}}{2 \cdot i_{d3}} \]
Inverter with variable capacitive output impedance (transistor $M_4$ & $M_8$)

Bias circuit is not necessary.

Control voltage $V_{ctrl}$ polarize gates transistors $M_3$ & $M_7$ which work in linear mode (like resistors) and determine output impedance.

It consists of:
- inverter stage
- variable capacitive load
Differential delay elements use limited charge/discharge current and parasite output capacitance to obtain delay.

Delay elements with differential input/output:
- Latch structure
- Good resistance on interference and compliance of rising and falling edge delay

Very fine delay regulation and good resistance to noise.
Complex realization, large power consumption, small output voltage level.
Current starved delay element has the best features:

- the wider range of delay regulation,
- simple realization,
- low-power consumption.
Delay Locked Loop (DLL)

DLL circuits is used for control delay elements and lines.

Ensures that the output clock signal to synchronize with a reference clock.

DLL architectures is classified into three types:

- analog
- digital
- hybrid (with double loop)

If exist, phase error between referent and output signals, negative feedback loop corrected delay value.
Delay
TIME RESPONSE
analogPDLL
digitalPDLL

(a)

Delay $t_d$
Time $t$

$T_{ref}$
$\Delta r$

CLK$_{ref}$
CLK$_{out}$

Voltage Controlled Delay Line
VCDL

Low-Pass Filter
CP

Current Pump
PD

CLK$_{ref}$
CLK$_{out}$

Digital Controlled Delay Line
DCDL

Finite Automat
Phase Selector

PD

TIME RASPONSE
digital DLL
analog DLL
HYBRID DLL

- the wider range of delay regulation
- fine regulation
- complex realization
- complex control
- larger power consumption
first order system, absolute stable

\[
\begin{align*}
    D_0(s) &= \frac{k_{PD} \cdot k_{CP} \cdot k_{DL}}{sC} = \frac{1}{1 + k_{PD} \cdot \frac{k_{CP}}{sC} \cdot k_{DL}} \\
    D_1(s) &= 1 + s \cdot \frac{C}{k_{PD} \cdot k_{CP} \cdot k_{DL}} \\
    H_{DLL}(s) &= \frac{D_0(s)}{D_1(s)} = \frac{1}{1 + s \cdot \frac{C}{f_{ref} \cdot I_{CP} \cdot k_{DL}}} = \frac{1}{1 + s / \omega_N} \\
    \omega_N &= \frac{k_{PD} \cdot k_{CP} \cdot k_{DL}}{C} = \frac{f_{ref} \cdot I_{CP} \cdot k_{DL}}{C}
\end{align*}
\]
second order system, potential unstable

\[ H_{PLL}(s) = \frac{\theta_0(s)}{\theta_i(s)} = \frac{K_{PD} \cdot K_{CP} \cdot K_{VCO} \cdot F(s)}{s + K_{PD} \cdot K_{CP} \cdot K_{VCO} \cdot F(s)} \]

\[ H(s) = \frac{\theta_0(s)}{\theta_i(s)} = \frac{2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2}{s^2 + 2 \cdot \xi \cdot \omega_n \cdot s + \omega_n^2} \]

\[ \xi = \frac{1}{2} \frac{\omega_n \tau_z}{2} \quad \omega_n = \sqrt{K_{PD} \cdot K_{CP} \cdot K_{VCO} \cdot K_F} \]
### Comparison of DLL and PLL

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>DLL</th>
<th>PLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency multiplying</td>
<td>No</td>
<td>yes</td>
</tr>
<tr>
<td>Architecture</td>
<td>simple</td>
<td>complex</td>
</tr>
<tr>
<td>transfer function</td>
<td>firs order</td>
<td>second order</td>
</tr>
<tr>
<td>stable</td>
<td>absolute</td>
<td>conditional</td>
</tr>
<tr>
<td>locking time</td>
<td>short</td>
<td>long</td>
</tr>
<tr>
<td>delay range of regulation</td>
<td>limited</td>
<td>unlimited</td>
</tr>
<tr>
<td>tracking jitter</td>
<td>small</td>
<td>large</td>
</tr>
</tbody>
</table>

- **Ring oscillator**: A basic circuit that generates a periodic waveform.
- **Delay Line**: A sequence of delay elements that can be used to create a delay in the signal path.

\[
\Delta t_{PLL}^2 = \frac{\omega_{ref}^2}{2 \omega_{PLL}}
\]

\[
\Delta t_{VCO}^2 = \alpha^2 \cdot \Delta t_{DLL}^2
\]

\[
\Delta t_{DLL}^2 = N \cdot \Delta t_d^2
\]
The proposed three solutions to the analog voltage controlled lines with linear regulation of the delay as a function of control voltage:

- With control threshold voltage
- Current starved delay element with symmetrical load
- Current starved element with nonlinear bias circuit

Proposed solutions differ in:

- Method of implementation
- Is useful for different range of delay regulation
Delay is determined by:
- charge/discharge current
- output impedance (capacitance)
- threshold voltage (hysteresis)

\[ t_{d_{LH}} = \frac{C}{I_1} (V_{H+} - V_-) \quad t_{d_{HL}} = \frac{C}{I_2} (V_+ - V_{H-}) \]

\[ \tau = \frac{C}{I} \Delta V \]

\[ \tau = t_{d_{LH}} = t_{d_{HL}} \]

\[ \Delta V = V_{H+} - V_- = V_+ - V_{H-} \]

\[ I_1 = I_2 = I \]
Delay regulation

Delay is proportional:
- output capacity and
- threshold voltage (hysteresis)
and reciprocal:
- charge/discharge output current

charge/discharge current

voltage controlled capacitance can not be implemented in linear and suitable manner
It consists of:

- integrator (IN)
- threshold voltage generator (GH)
- comparator (K)

Threshold voltage $V_H$ has opposite value for rising and falling clock edge, to avoid changes in pulse width.
scheme of delay line with hysteresis voltage regulation

realizacija analogne linije za kašnjenje sa regulacijom napona praga

hysteresis voltage generator with characteristic

$V_{ctrl}$ $V_{H+}$ $V_{H-}$ $V_{out}$

$V_B$ $M_6$ $M_7$

$V_{bp}$ $V_{bn}$ $C=1\text{pF}$

$M_1$ $M_2$ $M_3$ $M_4$ $M_5$ $M_6$ $M_7$

$CLK_{in}$ $CLK_{out}$

$V_{H+}$ $V_{H-}$ $V_H$

$M_{12}$ $M_{10}$ $M_9$ $M_8$

$V_+$ $V_{ctrl}$

$SW_1$ $IN$ $I_1$ $I_2$

$V_-$
Delay linearity error in function of control voltage.

Delay in function of control voltage.

Delay linearity error in function of control voltage.
The modification is made by adding transistors $M_5$ & $M_6$. They present symmetrical load.

Symmetrical load increases the current charging/discharging the output capacitance and changes the shape of the regulation characteristic. Current is a variable and its value depends on the output voltage. Symmetrical load provides negative feedback, which gives a linear regulation characteristic.
current starved delay element with symmetrical load

delay linearity error in function of control voltage

Delay in function of control voltage
The analytical model of the current starved delay element with symmetrical load is given by:

\[-C_L \frac{dV_0}{dt} = i_{d3} + i_{d5}\]

The delay \( t_{p1} \) is given by:

\[t_{p1} = \frac{\tau}{\sqrt{\frac{k_1}{k_2}(V_g - V_t)}} \cdot \arctan \left( \frac{k_1}{k_2} \frac{V_g - V_t}{\left( \frac{V_{dd}}{2} - V_t \right)(V_{dd} - V_t)} \right)\]
CURRENT STARVED DELAY ELEMENT WITH NONLINEAR BIAS CIRCUIT

Bias circuit control charging/discharging current $I_{cp}$ of output $C_{load}$ capacitance.

Typical, current $I_{cp}$ in a linear way depends on the control voltage $V_{ctrl}$. 

Interconnection of BIAS circuit and current starved element

The delay is determined by the equation:

$$t_d = \frac{C_{load} \cdot V_{dd}}{2 \cdot I_{cp}}$$
Nonlinear bias circuits use square characteristics of MOS transistor in saturation.

Bias circuit is designed to provide reciprocal relation between current and voltage.
Simulation of: bias circuit and current starved delay element

BIAS circuit simulation

Simulation of:

bias circuit and current starved delay element
DLL with two current pump. It provides differential control voltage.

**Bias circuit**

**CP1**

**LPF1**

**CP2**

**LPF2**

**VCDL**

**Voltage Controlled Delay Line**

**Four-stages delay line with nonlinear bias circuit**

**Charge Pump**

**Charge Pump**

**Phase Detector**

**DLL with current starved delay line and nonlinear bias circuit**

**Delay Line**
Simulation of DLL with two charge pump and nonlinear bias circuit
DLL and delay lines include wide area of applications:

- fast RAM memory,
- serial USB2 and IEEE 1394 interfaces
- FPGA chips,
- telecommunication,
- circuits for PN coda tracking
- spread spectrum systems
- measuring and processing equipment...

Some suggested applications:

- multi-frequencies and multi-phases clock synthesis with DLL
- high-resolution time-to-digital converter
- adaptive duty cycle corrector
The most important DLL's application is achieving the correct transfer data between two synchronous digital blocks, synthesis and distribution of clock signal, clock-skew and jitter problems elimination.
Multi-frequency and multi-phase clock synthesis with DLL

[Diagram of clock synthesis system]

- Phase Detector
- Current pump
- Loop Filter
- Delay Line
- Edge Combiner Circuit

Clock references (CLK_ref) and clock outputs (CLK_out) are shown with waveforms. The diagram illustrates the interaction between different phases and control signals, highlighting the synthesis process.
DLL based frequency multiplier uses voltage-controlled delay elements which represents a significant advantage related to the standard solution with a PLL frequency multiplier circuit which uses voltage controlled ring oscillator.

PLL and DLL Jitter

Illustration form of jitter accumulation in PLL and DLL circuits for frequency multiplying.
**high-resolution Time-to-Digital Converter**

The timing resolution of the delay Vernier technique is determined by the difference between two propagation delay values.

Start signal spreads through the upper (slower) delay line (\(t_{d1}\)).

Stop signal is spread through the lower (faster) line delay (\(t_{d2}\)).

Measurements resolution of several tens of pico-seconds can be achieved if difference in delays between upper and lower elements small enough.

Measurement range is equal to the duration of one period of reference clock.
DLL is used for calibration delay lines in Vernier convertora.

Implementation of Time-to-Digital Converter

Modifying Vernier delay technique

Fazni detektor

Strujna pumpa
Waveform of $S_i$ and $C_i$ represent *start* and *stop* pulses on outputs of appropriate delay elements.
Duty Cycle Corrector

Working principle of duty cycle corrector is based on delay element which gives a different delay value for rising and falling edge of signal.

Circuit from Fig. (c) has the widest range of regulation.

Circuits from Fig. (a), (b) and (d) have influence or just on expansion or just on compression of pulses.
Pseudo inverter control stage

(a) Scheme
(b) Equivalent scheme

Pulse/period ratio in function of control voltage $V_{\text{ctrl}}$
Spice simulation for different values of control voltage $V_{ctrl}$

**input and output waveform at pseudo inverter control stage**
Symmetrical relation between pulse/pause is unmatched when:

- signal passes through a long series of buffers,
- unbalance of N and P MOS transistors,
- technology variations,
- temperature or supply voltage have changed...

PWCL scheme

Waveform at PWCL obtained by Spice simulation
CONCLUSION

It is presented three new solutions for linear analog delay line:
- with threshold voltage control,
- with symmetrical load,
- with nonlinear bias circuit,

and proposed new and modified existing application:
- multi-frequency and multi-phase clock synthesis with DLL
- time-to-digital converter
- adaptive pulse width control loop

The applied models and design rules are for technology companies
South Africa Microelectronics (SAMES)