OFDM Data Transmission System in 60 GHZ spectrum range

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Overview

1. Frequency Regulation and Standardization
2. PHY Parameters
3. Phase Noise Modelling
4. 60 GHz Receiver and Transmitter Circuits
5. 5 GHz TX/RX
6. Baseband Processor
7. Demonstrator Architecture
8. Measurement Results
9. Conclusions
Frequency Regulation and Standardization

- Large amount of bandwidth available worldwide (3.5 to 7 GHz)
- TX-Power 10 dBm (40 dBm EIRP) allowed in most regions
- European regulation is in progress

IEEE802.15.3c Standard
- Proposal Presentation took place 05/2007
- Downselection started 07/2007
- Standard released in mid-2008
60 GHz OFDM PHY Parameters (1)

• Main application scenario: HDTV video streaming
• Narrowband (FFT-BW: 400 MHz) and wideband (FFT-BW: 800 MHz) PHY mode defined
• Standard convolutional (171,133) codes used
• Application of parallel coding streams allows implementation with low digital clock frequency
• Modulation ranges from BPSK-1/2 to 64-QAM-3/4
• Proposed 11-symbol long preamble for reliable synchronization
## 60 GHz OFDM PHY Parameters (2)

### Narrowband parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Subcarrier spacing</th>
<th>Symbol duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFT bandwidth</td>
<td>400 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FFT size</td>
<td>256</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Subcarrier spacing</td>
<td>1.5625 MHz</td>
<td></td>
<td>800 ns</td>
</tr>
<tr>
<td>Data subcarriers</td>
<td>192</td>
<td></td>
<td>160 ns</td>
</tr>
<tr>
<td>Pilot subcarriers</td>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Zero subcarriers</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cyclic prefix</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Wideband parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Subcarrier spacing</th>
<th>Symbol duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFT bandwidth</td>
<td>800 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FFT size</td>
<td>512</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Subcarrier spacing</td>
<td>1.5625 MHz</td>
<td></td>
<td>800 ns</td>
</tr>
<tr>
<td>Data subcarriers</td>
<td>384</td>
<td></td>
<td>160 ns</td>
</tr>
<tr>
<td>Pilot subcarriers</td>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Zero subcarriers</td>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cyclic prefix</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Baseband noise filtering (CPE correction): reduces phase noise at low offsets, especially efficient for short OFDM symbols length $T_u$.

Rms phase error:
$< 3$ degree for 16 QAM OFDM!

VCO phase noise:
$-95$ dBc/Hz at 1 MHz required, challenge for Si-based VCOs.

OFDM symbol length:
$T_u < 1 \mu s$ required for efficient phase noise filtering.

$$S_{eff}(f) = S_{PLL}^{out}(f) \times \left[1 - \sin c^2(fT_u)\right]$$

$$\sigma_\phi [\text{deg}] = \frac{180^0}{\pi} \sqrt{\frac{B^2}{2} \int_0^B 2S_{eff} df}$$
60 GHz Receiver Architecture

- **Vivaldi Antenna**
- **60 GHz LNA & Down-mixer**
- **5 GHz Quadrature Demodulator**
- **SMA-Connectors to ADC board**
- **Crystal 110 MHz**
- **Crystal 5 MHz**
- **Rogers 3003 Material**
- **Cavity**
- **IHE – Uni Karlsruhe**
60 GHz Receiver Chip (for 5 GHz IF)

Technology:
- 0.25 um SiGe BiCMOS
- $f_T / f_{max} \sim 200$ GHz
- $BV_{CEO} = 1.9$ V

Measurements:
- Gain ripple: $<1$ dB @ 57-64 GHz
- Simulated noise figure: 7.2 dB
- 0.8 mm$^2$ with bond-pads

Graphs showing:
- Conversion gain vs RF Frequency (GHz)
- LO fixed at 55 GHz
- IF fixed at 5 GHz

Chip photo
60 GHz Transmitter Chip

- Input 1-dB: -18 dBm
- ≈0 dBm output power

Chip photo and architecture (top)
5 GHz TX/RX

- PLL for I/Q generation is fully integrated with the quadrature mixer
  - For I/Q generation, SiGe bipolar divide-by-two circuits (DTC) are used
  - Quadrature mixer consists of two linearised Gilbert mixers
- Output spectrum of the upconverter: Spur level at -70 dBc
- Phase noise @ 1 MHz offset is -112 dBc/Hz
Baseband processing

• We have used high-speed FPGA development board

• Transceiver is fully verified for various channels and SNR ratios in simulation

• Transceiver is synthesized and mapped to the FPGA
   The baseband processor is tested without/with 60 GHz RF link

• Baseband link achieves 36 dB SNR
   Using the full RF 60 GHz link we have achieved the rate of 1080 MBit/s with 64-QAM
Basic Operating Scheme

- We use a modified and extended preamble structure to allow robust synchronization with low complexity.
  The preamble is extended to eleven OFDM symbols.

- System must allow the transmission of long frames, hence must track the time varying channel.
  We employ dual-mode operation to facilitate simple re-estimation of the channel coefficients.

- After every N normal data symbols, we insert 4 reference data symbols.
  Reference symbols are restricted to BPSK or QPSK.

- Original data stream is divided into several streams.
  Each stream should be terminated with a zero byte not only at the end of the frame but also in the reference symbols.

\[
\begin{array}{cccccccccc}
1 & 2 & 3 & 1 & 2 & 3 & 1 & 2 & 3 & 1 & \{\text{EOF}\}
\end{array}
\]

16-QAM 1/2  QPSK 3/4  \(T = \text{stream termination}\)

New reference

\[
\begin{array}{cccccccccc}
T & T & T & T & T & T & T & T & T & T & T
\end{array}
\]
Preamble Structure

14 short symbols (2.24 μs) for AGC

11 + 12 short symbols for frame detection, CFO estimation

4 long symbols channel estimation, time synchronization
Hardware Structure of the Baseband Processor

1. Input control block
2. Symbol calculation
3. Scrambler
4. Symbol mapping
5. Encoder 1
6. Encoder 2
7. Encoder 12
8. Interleaver 1
9. Interleaver 2
10. Interleaver 6
11. Interface
12. N_streams → 6
13. Interleaver 1
14. Interleaver 6
15. Subcarrier mapping and pilot insertion
16. Mapper
17. FFT 256
18. Preamble insertion
19. Symbol scheme buffer
20. Symbol scheme buffer
21. Signal field interpreter
22. Demapper/weighting
23. Deinterleaver 1
24. Decoder 1
25. Deinterleaver 2
26. Decoder 2
27. Deinterleaver 12
28. Decoder 12
29. Collect FIFO
30. Desramber
31. Data collector
32. Output interface
33. MAC
Synchronization and Channel Estimation

I/Q input signal $f_T = 800$ MHz

1. Decimation filter
2. Digital AGC
3. Synchronizer
4. Frontend controller
5. 256-Point FFT
6. FFT Shifter
7. Channel coefficients
8. Buffer (3)
9. Pilot Equalizer
10. Channel estimator
11. Phase unwrapper
12. Data Equalizer
13. Phase estimation
14. Data symbol extraction
15. Gate buffer (4)
16. Demapper / Routing
17. SF interpreter / global controller
18. De-Interleaver / Decoder 1

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## Hardware Complexity of Processor in FPGA

<table>
<thead>
<tr>
<th>block</th>
<th>gates (Mil.)</th>
<th>slices</th>
<th>flip-flops</th>
<th>4-input LUT</th>
<th>BRAM</th>
<th>MULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tx</td>
<td>7.8</td>
<td>12430</td>
<td>18069</td>
<td>16375</td>
<td>111</td>
<td>41</td>
</tr>
<tr>
<td>Rx</td>
<td>15.5 + 10</td>
<td>29142</td>
<td>27450</td>
<td>46632</td>
<td>225</td>
<td>56</td>
</tr>
</tbody>
</table>

+ indicates usage, ? indicates unavailable data.
Demonstrator Architecture

- High-speed FPGA board with add-on ADC/DAC modules
  - 8-bit dual A/D converters with a sampling rate of up to 1 GSps
  - 14-bit D/A converters with a sampling rate of 1 GSps

- The complete OFDM baseband transmitter was realized in hardware in the FPGA
  - The receiver algorithms were in this setup implemented in software
60 GHz Transceiver System

0.25 um SiGe BiCMOS Technology; Max data rate: 720 Mbit/s @ 500 MHz Bandwidth demonstrated
Measurement results

- Error free transmission demonstrated with 960 MBit/s, using Wideband PHY mode (800 MHz FFT-BW) and 16-QAM-1/2
- 100 frames with 2 kByte payload per frame evaluated
- Transmitter-receiver distance was around 20 cm (without PA)
Conclusions

• 60 GHz band offers unprecedented bandwidth allowing very high data rates

• For applications such as uncompressed HDTV transmission in a multipath environment, OFDM is a suitable and efficient modulation scheme

• SiGe BiCMOS technology is a suitable and cost efficient for high performance applications with multipath propagation

• Future 60 GHz ultra short range (LOS) systems will use single carrier modulation and RF circuits based on CMOS technology

• IEEE standardization will most probably define a 60 GHz PHY with two modes: single carrier and OFDM plus a common mode

• In 5 years from now, every other mobile phone will have a 60 GHz Gbit/s interface (if standardization doesn’t stall)
Acknowledgement

Thank you for your attention!

Acknowledgement:
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### High-Performance 0.25 µm SiGe:C BiCMOS (SG25H1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>npn1</th>
<th>npn2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bipolar Section</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$A_E$</td>
<td>$0.21 \times 0.84 \mu m^2$</td>
<td>$0.18 \times 0.84 \mu m^2$</td>
</tr>
<tr>
<td>Peak $f_{\text{max}}$</td>
<td>190 GHz</td>
<td>220 GHz</td>
</tr>
<tr>
<td>Peak $f_T$</td>
<td>190 GHz</td>
<td>180 GHz</td>
</tr>
<tr>
<td>$BV_{CE0}$</td>
<td>1.9 V</td>
<td>1.9 V</td>
</tr>
<tr>
<td>$V_A$</td>
<td>40 V</td>
<td>40 V</td>
</tr>
<tr>
<td>$\beta$</td>
<td>200</td>
<td>200</td>
</tr>
</tbody>
</table>
Scaling a current FPGA implementation the following figures can be estimated (4 data streams, 400 MHz digital CLK, 65 nm digital CMOS, 130 nm analog SiGe-BiCMOS assumed!):

- MAC Processor: 10 mm$^2$ (ca. 10 Mio Gates)
- Baseband Processor: 15 mm$^2$ (ca. 15 Mio Gates)
- Data Converters: 10 mm$^2$
- Analog Frontend (incl. PA): 6 mm$^2$

Size Complete Transceiver PCB: 5 cm x 4 cm x 3 cm
Size of Antenna (Patch Array): 30 mm x 40 mm x 2 mm
Back-up 2: Estimated Power Dissipation

- **Total Power Dissipation at 2 Gb/s**
  (65 nm CMOS digital; 130 nm analog SiGe)

<table>
<thead>
<tr>
<th>Component</th>
<th>TX</th>
<th>RX</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAC Processor</td>
<td>200 mW</td>
<td>200 mW</td>
</tr>
<tr>
<td>Baseband Processor</td>
<td>200 mW</td>
<td>350 mW</td>
</tr>
<tr>
<td>Data Converters</td>
<td>100 mW</td>
<td>150 mW</td>
</tr>
<tr>
<td>Analog Frontend</td>
<td>200 mW</td>
<td>200 mW</td>
</tr>
<tr>
<td>Power Amplifier</td>
<td>150 mW</td>
<td>20 mW</td>
</tr>
</tbody>
</table>

- **Total (continuous):**
  850 mW 920 mW