Architecture of a Power-Gated Wireless Sensor Node

Abstract — In this paper we investigate the benefits of power-gating in wireless sensor nodes operating at a very low duty cycle. It is shown that the static power loss in such a node is significant portion of the total power consumption. Therefore, we have designed a power-gated wireless sensor node architecture and developed a power-gating mechanism to reduce the static power loss of its functional blocks. The new node architecture, its components and power-gating mechanism are described in detail.